



UNITED STATES DEPARTMENT OF COMMERCE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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[REDACTED] EXAMINER

[REDACTED] ART UNIT PAPER NUMBER

[REDACTED] DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)
	09/585,261	LOH, KAH PHANG
	Examiner Tuan T Dinh	Art Unit 2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 10 September 2001.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-7 and 10-12 is/are pending in the application.
- 4a) Of the above claim(s) 8 and 9 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-7 and 10-12 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 02 June 2000 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____

- 4) Interview Summary (PTO-413) Paper No(s) _____
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____

DETAILED ACTION

Applicant's election of **Group I in Paper No. 5** is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been **treated as an election without traverse (MPEP § 818.03(a)).**

Drawings

Figures 1-5 should be designated by a legend such as --**Prior Art**-- because only that which is old is illustrated. See MPEP § 608.02(g).

Claim Objections

Claim 1 is objected to because of the following informalities:

Claim 1, line 4, after "side surface" insert --said planar circuit board--

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless —

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-7 and 10-12 are rejected under 35 U.S.C. 102(a) as being anticipated by Fujii (U. S. Patent 6,023,414).

As to claim 1, Fujii discloses a circuit board assembly as shown in figures 1-7 comprising:

a planar circuit board (2, column 4, line 5) having a major surface and a side surface (see figure 3);

a planar substrate (12, column 3, line 16) mounted on the major surface of the circuit board, an extended portion of the planar substrate extending beyond the side surface; and

a substrate (13, column 1, line 32) consider as an optical transceiver module mounted on the extended portion of the substrate (12) adjacent the side surface of the printed circuit board (2-figure 3-4).

As to claim 2, Fujii discloses a circuit board assembly as shown in figures 3-4 wherein the planar circuit board (2) includes an end portion defining a recess (20, column 4, line 9) in which the optical transceiver module (13) is disposed.

As to claim 3, Fujii discloses a circuit board assembly as shown in figures 1-7 wherein the planar substrate (12) includes electrically conductive interconnects (12d, column 4, line 30) for coupling electrical terminals on the optical transceiver module with electrical terminals on the planar circuit board.

As to claim 4, Fujii discloses a circuit board assembly as shown in figure 4 wherein the planar substrate (12) and the planar circuit board (2) are substantially parallel.

As to claim 5, Fujii discloses a circuit board assembly as shown in figures 1-7 wherein the planar substrate is soldered onto the major surface of the planar circuit board (column 4, lines 29-31).

As to claim 6, Fujii discloses a circuit board assembly as shown in figures 1-2 wherein the optical transceiver module is soldered onto the extended portion of the planar substrate.

As to claim 7, Fujii discloses a circuit board assembly as shown in figures 3-7 wherein the optical transceiver module is mounted on, and the major surface of the planar circuit board faces a same side of the planar substrate.

As to claim 10, Fujii discloses a circuit board assembly as shown in figures 1-7 comprising:

`a planar circuit board (2) having a major surface, and a side surface defining a recess (20);

a planar substrate (12) mounted on the major surface of the circuit board (2), an extended portion of the planar substrate extending over the recess (see figure 4); and

an optical transceiver module (13) mounted on the extended portion of the substrate (12) so as to be disposed in the recess (20) of the circuit board.

As to claim 11, Fujii discloses an optical transceiver module package (1) for mounting on a planar circuit board (2-figures 3-7) having a major surface and a side surface, the major surface provided with electrical terminals (21), the optical transceiver module package as shown in figures 1-7 comprising:

a planar substrate (12) for mounting on the major surface of the circuit board (2) so that an extended portion of the planar substrate (12) extends beyond the side surface (see figure 4);

an optical transceiver module (13) provided with electrical terminals and mounted on the extended portion of the substrate (12) adjacent the side surface of the printed circuit board; and

electrically conductive interconnects (12d) associated with the planar substrate for coupling the electrical terminals on the optical transceiver module (13) with electrical terminals (21 on the planar circuit board (2).

As to claim 12, Fujii discloses an optical transceiver module package (1) as shown in figures 1-7 comprising:

a planar substrate (12) for mounting on the major surface of a circuit board (2) so that an extended portion of the planar substrate extends over a recess (20) of the circuit board;

an optical transceiver module (13) provided with electrical terminals and mounted on the extended portion of the substrate (12) so as to be disposed in the recess; and

electrically conductive interconnects (12d) associated with the planar substrate (12) for coupling the electrical terminals on the optical transceiver module with electrical terminals (21) on the planar circuit board.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Verdiell, Shih et al., Kunii et al. Disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 703-306-5856. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 703-308-3301. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-3431 for regular communications and 703-308-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TD
September 28, 2001


Jayprakash N. Gandhi
Primary Examiner
Technology Center 2890